Nov 17

Dual Beam AO Modulator Driver

Including: Optical Alignment

DBM1330–aQ160-6
(for duty cycled operation ONLY, 20% max)

Instruction Manual (revision 6a)
iSPA2160-4 Series
Quad output RF Synthesizer and Amplifier

Models -

iSPA2160-4-xxx	: 160.0 MHz 4-channel phase steered, 24W total RF output (optimized for 355nm)

Options **–xxx**, combinations possible

- V	: 0-5V analog modulation range
- BR	: Brass water cooled heatsink

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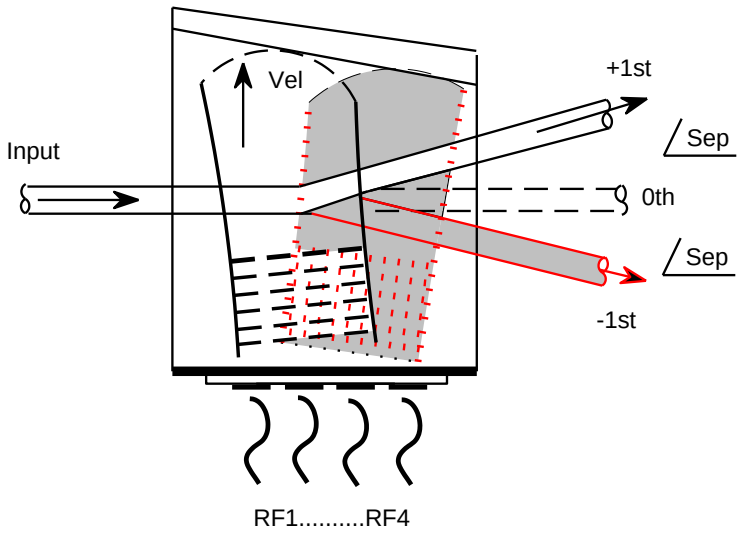
Revision History

21-4-11	Test point output on D-type. RF envelope provided for timing purposes during set-up
1-10-12	Correction to manual. Digital inputs are LVTTL. Protection circuitry will clamp 5V logic level inputs to 3V3. Recommended maximum logic HIGH voltage is 3V3.
17-3-13	Re-labelled –OHL input from P0 to P3. Pin assignment unchanged
17-3-13	Addition of RF blanking input –RFB on pin 3.
12-11-13	Modify logic and protection diodes for 5V logic Note: -RESET and –RFB still use internal pull-up resistors to 3V3. These signals should be driven with open-collector circuits.
06-11-17	Added pulse picking method. and duty cycle warnings for DBM1330-aQ160

1. GENERAL

The iSPA range of configurable RF drivers is based on a quad channel RF synthesizer and 16-bit MCU. The MCU contains non-volatile FLASH memory for program storage. This enables the operating characteristics of the driver to be loaded at power-on without user intervention. The MCU also provides diagnostic and house keeping capabilities.

The iSPA drivers are typically programmed at the factory for a specific OEM application.
The remainder of this manual will describe the iSPA2160-4 variant. These drivers use bi-level phase modulation to generate acoustic beam steering in an AO modulator. The result is a single AO device that can efficiently diffract the incoming laser beam into either the +1 or -1 first order angles without mechanical readjustment.



Key Features:

- Quad output, up to 5W per channel, water cooled power amplifier
- Microprocessor controlled RF synthesizer
- Fast switching and frequency selection times < 100nsec
- High speed digital and analog modulation
- RF blanking
- Independent power controls
- Tri colour LED status indicators

The iSPA2160-4 Combined Driver and Power Amplifier is a specifically designed to operate with the DBM1330-aQ160 series of dual beam acousto-optic high power modulators. A block diagram of the driver is shown in Figure 5. The 16-bit MCU features internal FLASH, RAM and a multi-channel ADC, plus USB, SPI and I2C interfaces. In normal use the driver is pre-programmed and will not require the USB connection to a host computer. All operational driver controls are through the 25 way D-type connector. On power up or after a Reset, the MCU configures the direct digital synthesizer (DDS) chip and loads a number of frequency / phase / amplitude profiles. These profiles can be rapidly selected via the Select input, P3 (and if applicable, P0 and/or P2). The frequency is accurate and stable to within ± 25ppm. Diode ring mixers provide RF level (analog) modulation of the RF carrier. The active controlling input (MOD_A or MOD_B) is also determined by the Select input P3 via a 4-way analog switch. Additional digital controls include:

-OHL: provides a fast ON:OFF Gate (Digital modulation) function.
-RFB: provides a global RF blanking or disable function.

The peak RF power level is factory set.
The output stages are Class A power amplifiers with fast rise and fall times.

2, CONTROL

Four inputs directly control the RF output; ***P3***, ***MOD_A***, ***MOD_B*** *and* ***-OHL***
The response time of either of these inputs is < 100nsec.
In addition the RF is enabled / disabled by the RF blanking input ***–RFB***
This is zero voltage input with internal pull- up resistor
The response time of the blanking input is < 2usec.

When connected to the DBM1330 series AOM:

P3: Selects which output beam is diffracted, +1 order or -1st order. This is achieved through phase reversal of the four RF inputs to the AOM (see Fig 1)
MOD_A: Sets the power level of the diffracted 1st order beam when P3 = 0
MOD_B: Sets the power level of the diffracted 1st order beam when P3 = 1
-OHL: provides ON:OFF control for both 1st order beams when P3=0 or P3=1
-RFB: Enables the RF, all outputs.(open collector driver required)

The relationship between the driver control inputs, the RF waveform and AO response is illustrated in the following diagrams.

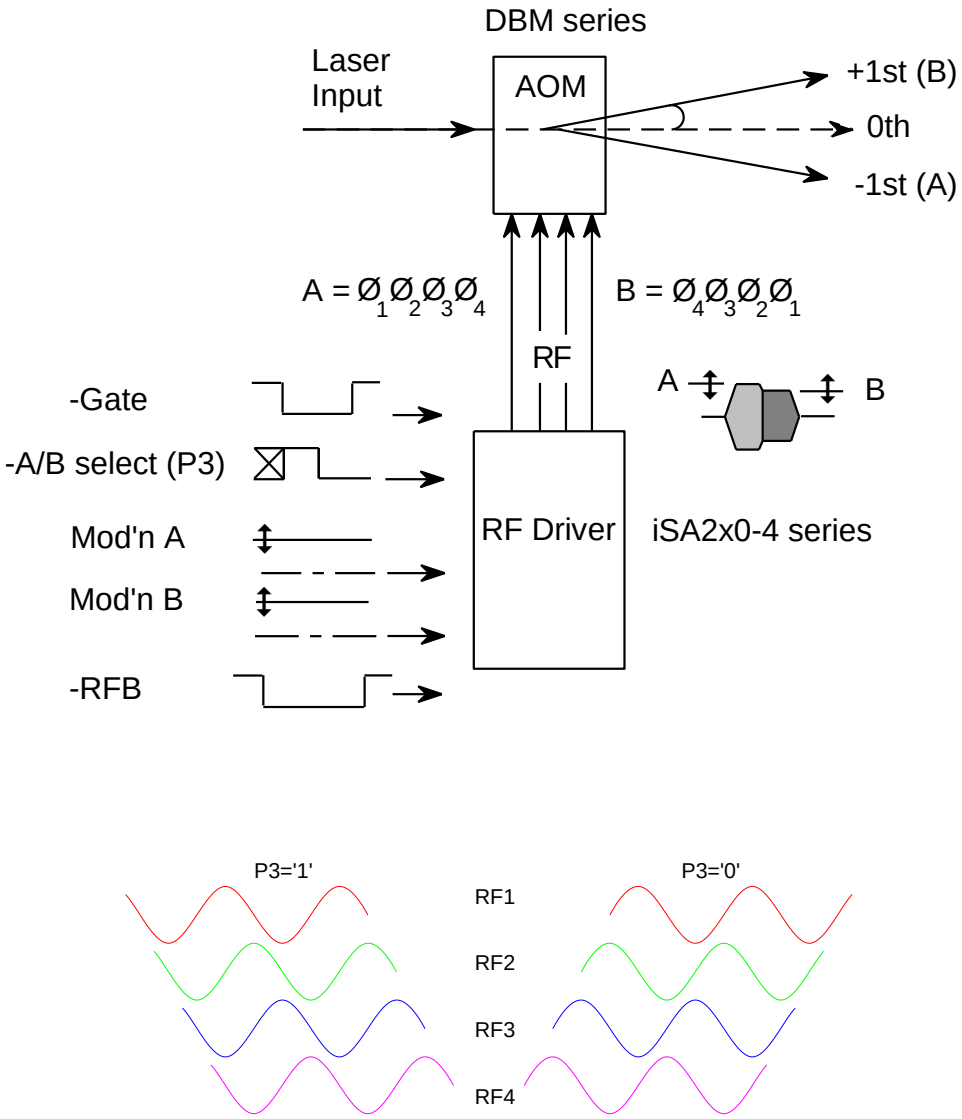


Fig 1: Phase Control

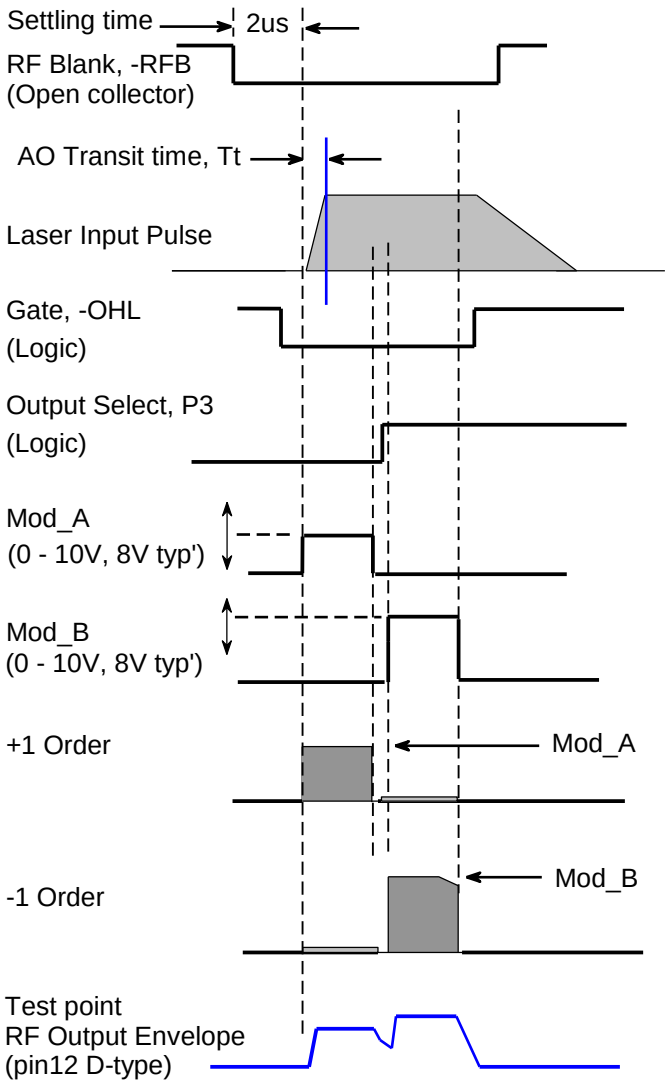
There are various methods to generate modulated pulses.

All have independent power control for the +1 and -1 beams.

The pulse shapes below are for illustrative purposes.

2.1 Method A (analog modulation, pulse width division)

- Modulation inputs (MOD_A and MOD_B) control the pulse amplitudes
- Modulation inputs (MOD_A and MOD_B) also control the pulse widths
- Input P3 selects the '+1' or '-1' output
- Gate (-OHL) input controls the RF Active period pulse width



Logic levels are 5V-CMOS / TTL compatible, except –RFB

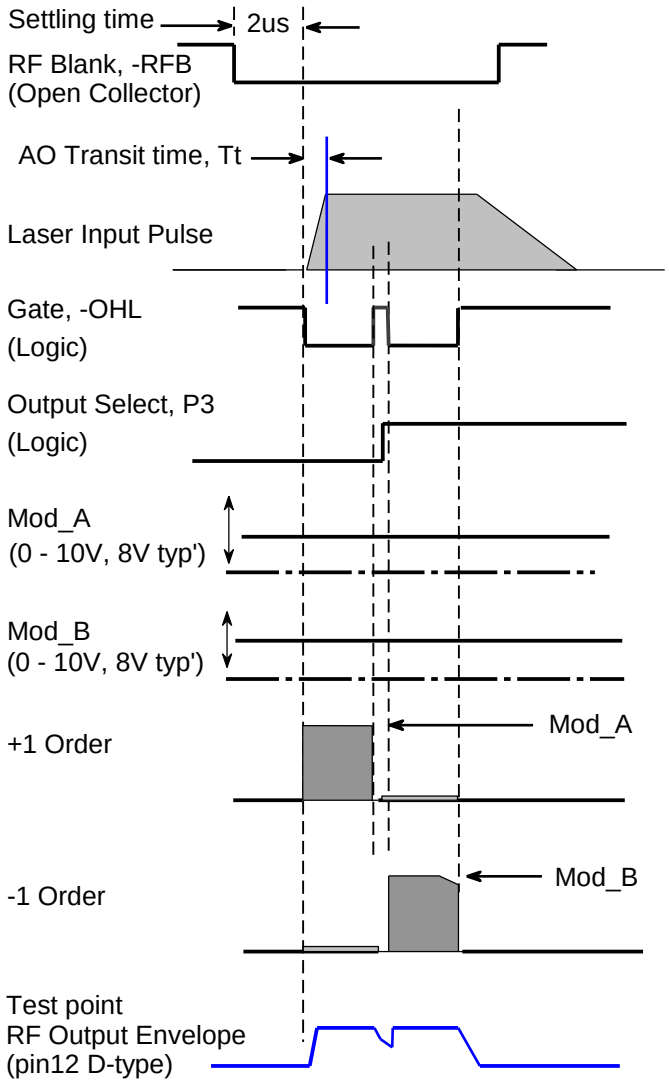
Notes: Mod_A and Mod_B signals shown at different levels for illustration purposes.

There will always be some residual power in the unselected "OFF" beam.
When correctly adjusted, this level should be less than 2% of the input power.

MAXIMUM RF duty cycle 20%
Refer to appendix A for timing explanation

2.2 Method B (digital modulation, pulse width division)

- Modulation inputs (MOD_A and MOD_B) control the pulse amplitudes only
- Gate (-OHL) input controls the output pulse width
- Input P3 selects the '+1' or '-1' output



Logic levels are 5V-CMOS / TTL compatible except -RFB

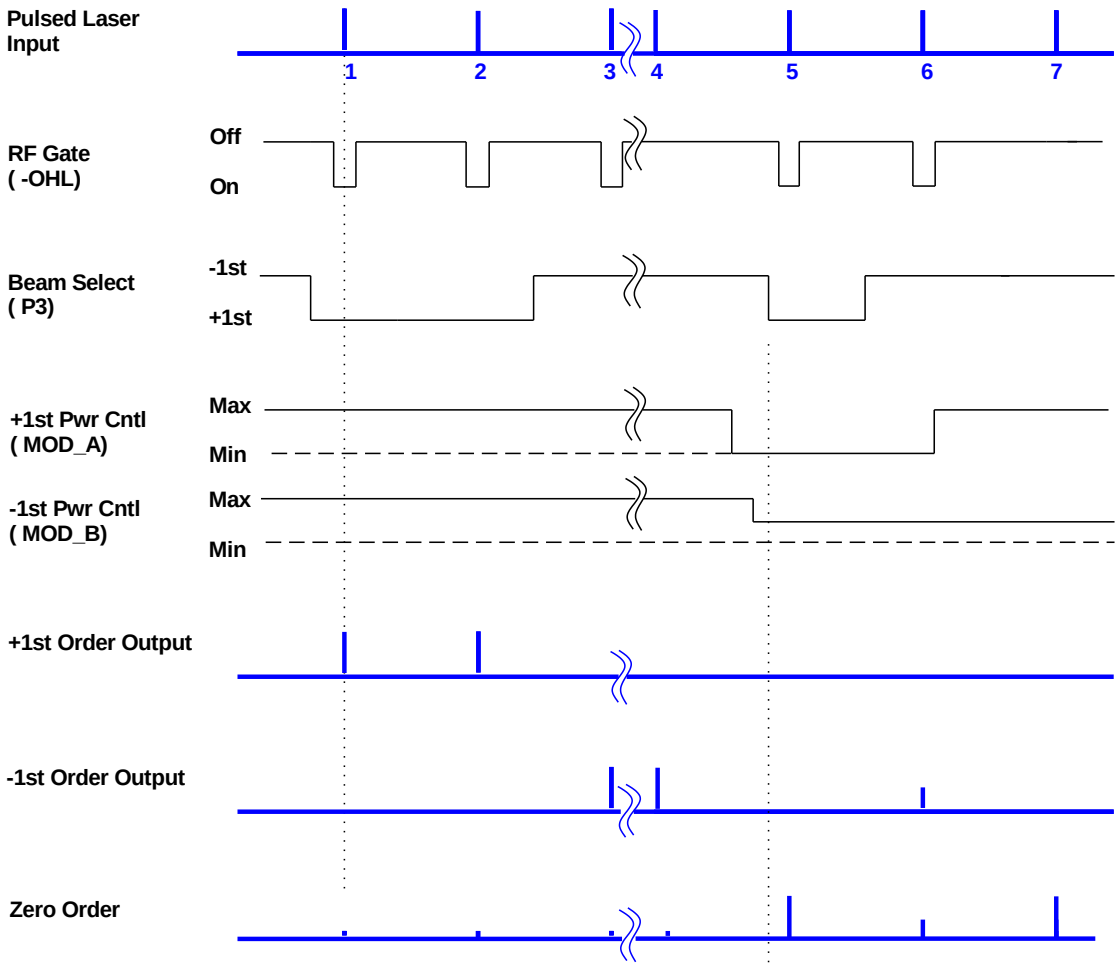
Notes: Mod_A and Mod_B signals shown at different levels for illustration purposes.

There will always be some residual power in the unselected "OFF" beam.
When correctly adjusted, this level should be less than 2% of the input power.

MAXIMUM RF duty cycle 20%
Refer to appendix A for timing explanation

2.3 Method C (digital modulation, pulse picking)

- Modulation inputs (MOD_A and MOD_B) control the pulse amplitudes only
- Gate (-OHL) input controls the active RF period i.e. duty cycle.
- Input P3 selects the '+1' or '-1' output
- -RFB permanently low in this example



Logic levels are 5V-CMOS / TTL compatible except -RFB

Notes: Mod_A and Mod_B signals shown at different levels for illustration purposes.

There will always be some residual power in the unselected "OFF" beam.
When correctly adjusted, this level should be less than 2% of the input power.

MAXIMUM RF duty cycle 20%
Refer to appendix A for timing explanation

2.4 Modulation characteristic

The +1 and -1 diffracted orders have the same modulation characteristics.

An illustration using Method A, analog modulation control is shown below

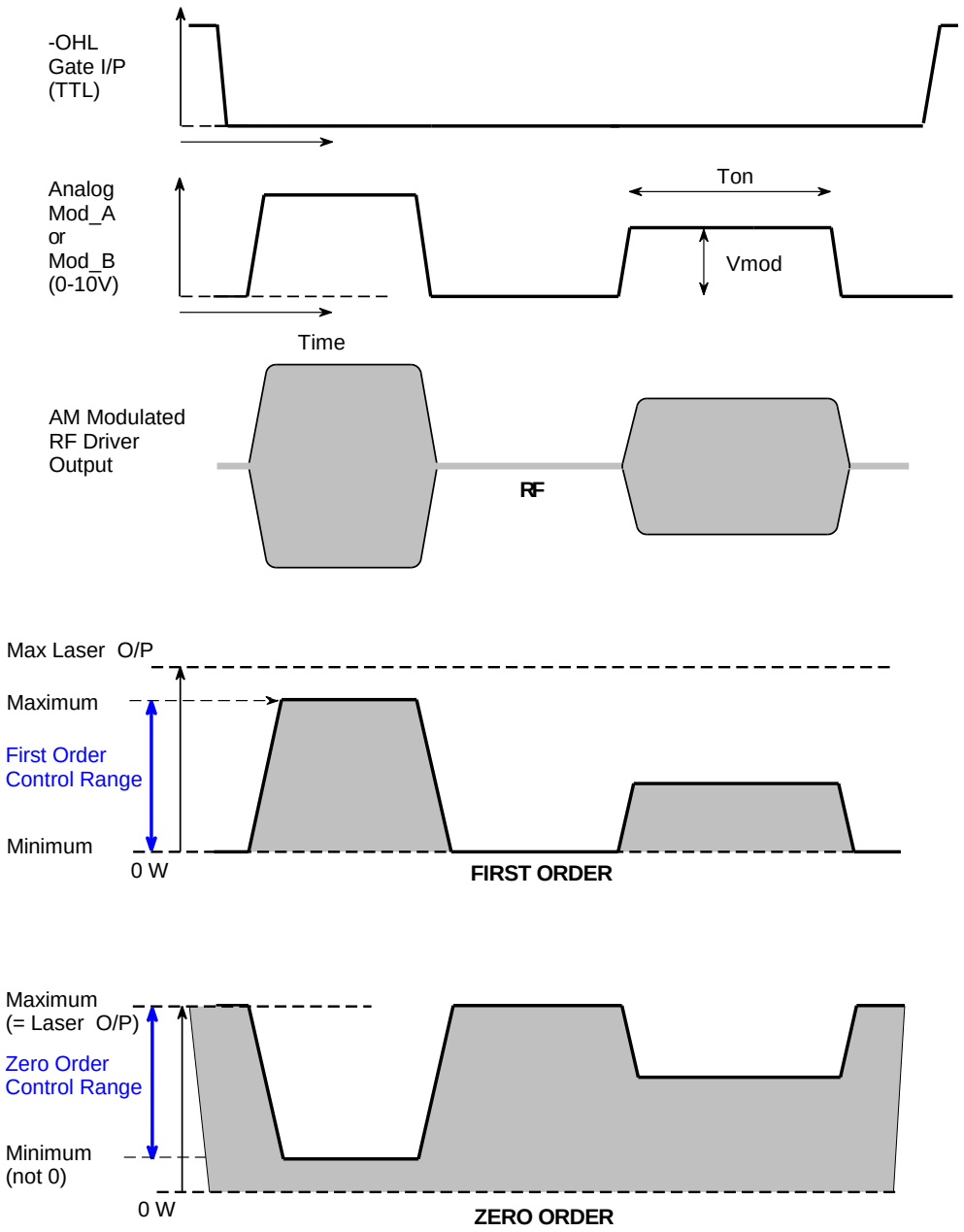


Figure 2: Typical Laser Modulation Waveforms

2.5 Signal Description

-OHL, Gate (active low switches RF On)

5V_CMOS/TTL compatible digital input

The default or 'not connected' condition is RF Off.

A high level (1.9V < V < **5V5**) will gate the RF **OFF**.

A low level (0V < V < 0.8V) will gate the RF **ON.**

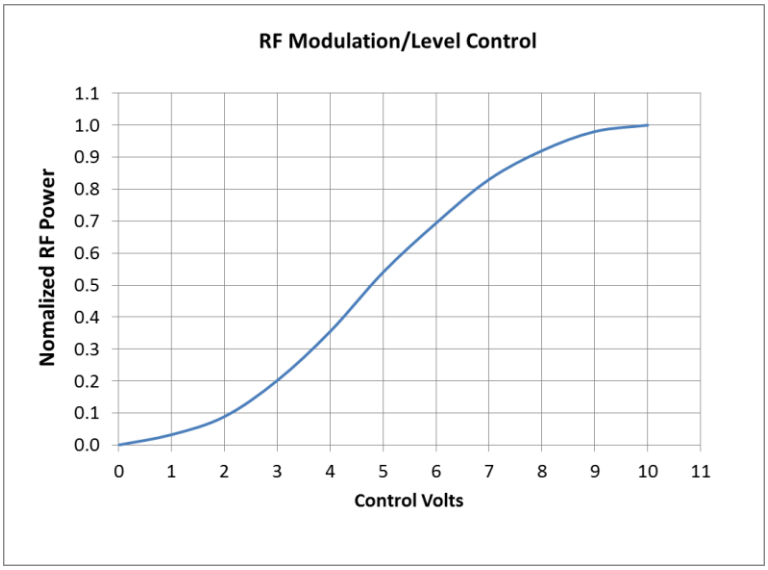
(For DBM1330-aQ1330, maximum RF On duty system = 25%)

Mod_A / Mod_B (Analog Modulation/RF Level inputs)

Provides high speed proportional amplitude control of the RF power.

Minimum RF output = 0.0V

Maximum RF output = 10.0V. (Normal operating level for maximum DBM efficiency is 7V – 9V)



Typical RF power characteristic per output

P3, Select

LVTTL 5V tolerant digital input

The default or 'not connected' condition is P3=1.

A high level (1.9V < V < 5V) will select phase order RF1-RF2-RF3-RF4 **and** Mod_B level control

A low level (0V < V < 0.8V) will select phase order RF4-RF3-RF2-RF1 **and** Mod_A level control

The relationship between the Phase order and the selected first order beam depends on the cable connection order and relative laser alignment. Refer Fig 7 for options.

-RFB, Blanking (active low enables the RF)

A no-voltage digital input. Internal pull-up to 3V3

If an active logic signal is connected, DO NOT exceed 3V3 on this input.

Open circuit or 'not connected' condition is RF Off.

Closed circuit (0V < V < 0.8V) will gate the RF **ON.**

The frequency settling time is approximately 1.5usec after –RFB is switched to a low level.

2.6 DC Power

A low impedance DC power supply is required. The operating voltage is +24Vdc only at a current drain of approximately < 4A. The external power source should be regulated to ± 2% and the power supply ripple voltage should be less than 200mV for best results. Higher RF output power is achieved at 28Vdc.

2.7 Thermal Interlocks

The AOM and Driver are fitted with thermostatic switches which will switch open circuit if a predetermined temperature is exceeded. These thermal interlocks will reset once the AO device and / or RF driver are cooled below this temperature*.

- The iSPA driver over-temperature threshold is 50deg C
- The DBM series over-temperature threshold is 40deg C

* The hysteresis of these thermal switches is 13deg C minimum.

Once in a fault state the coolant temperature will need to be reduced below 20degC to reset the thermal switches.

Precautions

- **Maximum RF ON duty cycle for the DBM1330-aQ160 is 25%**
- **-RFB and –Reset digital input levels must not exceed 3.3 volts**
- **In general, digital input levels must not exceed 5 volts, (unless specified)**
- **Analog logic input levels must not exceed 12 volts**

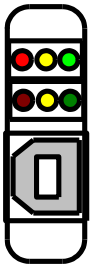
Water cooling is mandatory. The DBM or driver heatsink temperature must not exceed 50°C. Corrosion inhibitor must be added to the cooling water

SERIOUS DAMAGE TO THE AO DEVICE WILL RESULT IF THE TEMPERATURE EXCEEDS 70°C. SERIOUS DAMAGE TO THE AMPLIFIER MAY RESULT IF THE TEMPERATURE EXCEEDS 70°C. SERIOUS DAMAGE TO THE AMPLIFIER MAY ALSO RESULT IF THE RF OUTPUT CONNECTOR IS OPERATED OPEN-CIRCUITED OR SHORT-CIRCUITED.

2.8 LED Indicator and Monitor outputs

The two front panel tri-colour LED sets indicate the operating state.

LED1	A	B	C
LED2	D	E	F



RED - A

The top left LED will illuminate RED when DC power is applied

Normal condition is ON

YELLOW - B

The top middle LED will illuminate YELLOW when:

- Interlocks are enabled (INT = Low)
- Power amplifier stages are enabled

Normal condition is ON

GREEN - C

The top right LED will illuminate GREEN when the reflected RF power is below the fault threshold.

Threshold level is factory set

Normal condition is ON

RED - D

The bottom right LED will illuminate RED when there is a fault condition:

This signal is available on pin 8 of the D-type connector. See STATUS MONITOR below

Fault conditions:

- Poor VSWR load (High reflected RF power fault) on one of the outputs.

  A fault signal is triggered when the reflected RF power exceeds approximately 50% of the average forward power for more than 1 second. This fault is latching and the driver is disabled (RF power will go to zero). This fault can occur if the RF connection between the AOM and driver is broken

- DC power below 22Vdc
- Interlock fault, INT = not connected or AOM over temperature

Normal condition is OFF

YELLOW - E

The bottom middle LED will illuminate YELLOW when, when the DC input is > 22V

Normal condition is ON,

GREEN - F

The bottom left LED : Not used

Condition is OFF

RESETTING

Once the fault condition is corrected, it will be necessary to reset the driver.

1) Turn the DC power OFF and ON

or

2) RESET the driver by momentary connecting pin 13 of the D-type to pin 25

Status Monitor Output

The status of the RED-D LED is available at the D-type connector

"FAULT" = logic low between pins 8 and 21 = RED-D ON

"OK" = logic high between pins 8 and 21 = RED-D OFF

LVTTL compatible. Sink / Source 4mA

Test Point

An analog voltage representing the RF envelop is available on the D-type connector pin 12

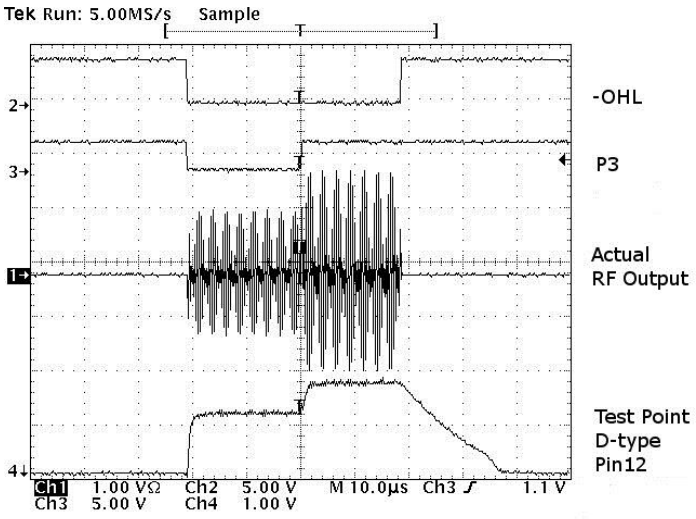
Return (0V) signal is on pin 25.

Use a 10Mohm scope probe only. Do NOT connect permanently.

This signal can be used to determine RF timing with respect to the laser pulse during set-up.

This signal is not a calibrated measure of the RF power level.

For clarity of image shot, the Mod_A and Mod_B inputs were set to give different RF power levels at P3=1 and P3=0



3. INSTALLATION and ADJUSTMENT

Refer to timing diagram in Appendix A

3.1 Connect cooling water to the iSPA2160-4 at a flow greater than 2.0 litres/minute at < 20 deg.C. Refer to Figure 2. Use of a Corrosion inhibitor is strongly advised.

Connect cooling water to the AO device.

Due to the high RF power dissipated in the AO modulator, it is paramount that the device is operated only when water cooling is circulating.

For optimum AO performance ensure the flow rate is more than 2 litres/minute at < 20 deg.C

3.1b Connect the + 24Vdc (4A continuous capability) to the screw terminals as marked.
DO NOT APPLY POWER.

3.2 Connect the four SMA output RF connectors to the four acousto-optic modulator SMA RF inputs (or a 50Ω RF load, if it is desired to measure the RF output power).
Connection order shown in Fig 7

3.4 Connect the Interlock of the acousto-optic modulator (mini 3-pin snap connector) to the RF driver “INT” input (mini 4-pin snap connector). Connections shown in Fig 3

3.5 If the temperature of the modulator exceeds 32ºC or the internal driver temperature exceeds 50ºC then the interlock connection becomes open circuit, disabling the RF output. An LED indicator illuminates when the Interlocks are closed and the RF is enabled.

3.6 Adjustment of the RF output power is best done with amplifier connected to the acousto-optic modulator. When shipped, the Amplifier output power is set to give 2W maximum per output.

3.7 The optimum RF power level required for the modulator to produce maximum first order intensity will be differ depending in the laser wavelength. Applying RF power in excess of this optimum level will cause a decrease in first order intensity (a false indication of insufficient RF power) and makes accurate Bragg alignment difficult. It is therefore recommended that initial alignment be performed at a low RF power level.

For the iSPA drivers, the RF power is adjusted by the Mod_A an Mod_B analog voltage levels

The set up procedure will select one first order beam at a time.
The initial alignment is made at half RF power (MOD_n = ~5V).

3.8 Apply DC to the amplifier

3.9 Apply a closed contact signal to the ***-RFB*** input. Connect pin 7 to pin 20 of the 25 way D-type.

3.10 Apply a 75% High, **25% Low** TTL pulsed signal to the ***-OHL*** input. Connect pin 7 of 25 way D-type to the TTL signal and pin 20 to the signal return (0V).

3.11 Apply a constant TTL **low** signal to the ***P3*** input. Connect pin 1 of 25 way D-type to the TTL signal and pin 14 to the signal return (0V).

3.12 Apply a constant analog input of 6V to both ***MOD_A*** and ***MOD_B***. Connect pin 5 (6) of the 25 way D-type connector to the Signal and pin 18 (19) to the signal return.

Input the laser beam toward the centre of either aperture of the AOM/DBM. Ensure the polarization is horizontal with respect to the base and the beam height does not exceed the active aperture height of the AOM/DBM. Start with the laser beam normal to the input optical face of the AOM/DBM. See Figures 6 & 7 for the possible configurations.

3.13 Observe the diffracted first-order output from the acousto-optic modulator and the undeflected zeroth order beam. Adjust the input angle (rotate the modulator) very slightly to maximise the first order beam intensity. Angle will be less than +/-10mrad

3.14 Apply a constant TTL **high** signal to the ***P3*** input.
This will select the other first order beam location

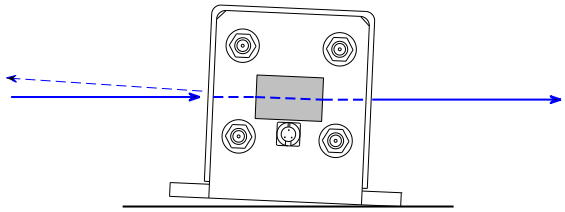
3.15 Again, observe the diffracted first-order output from the acousto-optic modulator and the undeflected zeroth order beam. If required, re-adjust the input angle (rotate the modulator) very slightly to balance the two first order beam intensities (i.e. switch between P3=0 and P3=1 and compare beam efficiencies)

3.16 After the input angle has been optimized, slowly increase the RF power by increasing MOD_A and MOD_B inputs until maximum balance first order peak intensities are obtained in both first orders

The peak efficiency value should occur between **7V to 9V.** The modulator and driver are now ready for use.

3.17 Back reflections

Unlike normal AO modulators, the DBM optical face is near normal to the incident laser beam. Depending on the optical design, there is a risk of back reflection into the laser cavity.
In such cases, it is recommended that the DBM is mounted at a slight angle to the horizontal, as shown below.



4. MAINTENANCE

4.1 Cleaning

It is of utmost importance that the optical apertures of the deflector optical head be kept clean and free of contamination. When the device is not in use, the apertures may be protected by a covering of masking tape. When in use, frequently clean the apertures with a pressurized jet of filtered, dry air.

It will probably be necessary in time to wipe the coated window surfaces of atmospherically deposited films. Although the coatings are hard and durable, care must be taken to avoid gouging of the surface and leaving residues. It is suggested that the coatings be wiped with a soft ball of brushed (short fibres removed) cotton, slightly moistened with clean alcohol. Before the alcohol has had time to dry on the surface, wipe again with dry cotton in a smooth, continuous stroke. Examine the surface for residue and, if necessary, repeat the cleaning.

4.2 Troubleshooting

No troubleshooting procedures are proposed other than a check of alignment and operating procedure. If difficulties arise, take note of the symptoms and contact the manufacturer.

4.3 Repairs

In the event of deflector malfunction, discontinue operation and immediately contact the manufacturer or his representative. Due to the high sensitive of tuning procedures and the possible damage which may result, no user repairs are allowed. Evidence that an attempt has been made to open the optical head will void the manufacturer's warranty.

Connection Summary

1.0 25 way 'D' Type Control Connection

	Type	Pin out connection
NECESSARY SIGNALS		
-RFB digital Blanking ** **Compatible with LVTTL open collector** Internal pull up to +3V3 via 4K7ohm Open (1.9v<V<**3v3**) = OFF Closed (0.0v<V<0.8v) = ON	Input	Signal pin 3 Return pin 16
-OHL digital Gate * CMOS/TTL High (1.9v<V<5v5) = OFF Low (0.0v<V<0.8v) = ON	Input	Signal pin 7 Return pin 20
P3 Select CMOS/TTL High (1.9v<V<5v5), P3= 1 Low (0.0v<V<0.8v), P3= 0	Input	Signal pin 1 Return pin 14
MOD_A (P3=0 selects) 0 – 10V max	Input	Signal pin 6 Return pin 19
MOD_B (P3=1 selects) 0 – 10V max	Input	Signal pin 5 Return pin 18
OPTIONAL SIGNALS		
'Status' monitor (LVTTL compatible, Low = Fault) Maximum current = 4mA	Output	Signal pin 8 Return pin 21
-RESET ** Active low. (0.0v<V<0.8v) = reset **Compatible with LVTTL open collector** Internal pull up to +3V3 via 10Kohm	Input	Signal pin 13 Return pin 25
RF Test Point (analog voltage)	Output	Signal pin 12 Return pin 25

Notes:

DO NOT connect to pins 9, 10, 11,
Pins 14 to 25 are internally connected to 0V
** Recommend zero-voltage contacts e.g. open collector drivers

Modulation and Gate Input connections

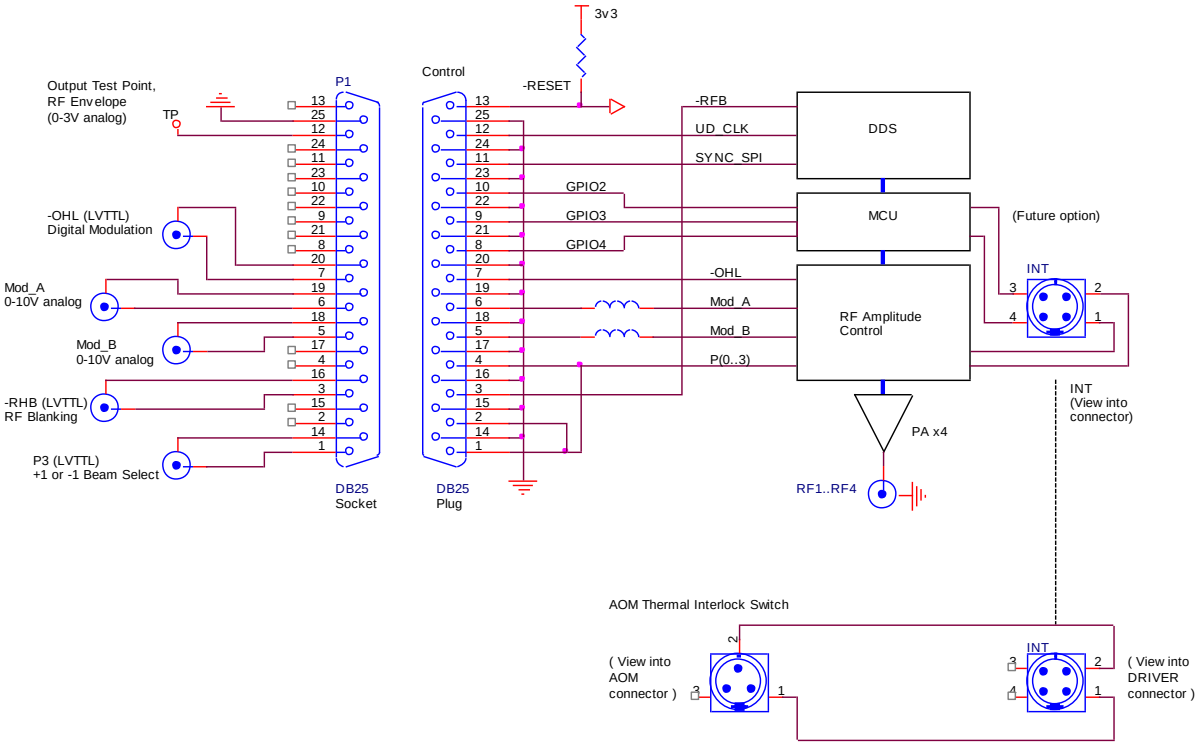
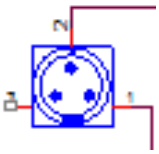


Figure 3:

2.0 Binder719 3-way Interlock Connector

Interlock *** Normally closed See Fig 3 Pin1 – Pin1 Pin2 - Pin2	Input	Connect to AOM “INT”



Do not connect remaining pin
(pin1 = first pin anticlockwise from largest gap, when looking into driver connector)

Notes:

* The digital Gate /Modulation input signal (pin 7) needs to be applied. This signal is active Low. It is required even if the analog inputs Mod_A and Mod_B are used to modulate the RF power.

** The RF Blanking input signal (pin 3) needs to be applied, This signal is active Low. Recommend zero-voltage connection e.g. open collector drivers or hardwire to 0V

*** The interlock signal must be connected. Contacts closed for normal operation.

3.0 Mounting Holes

4 x M5

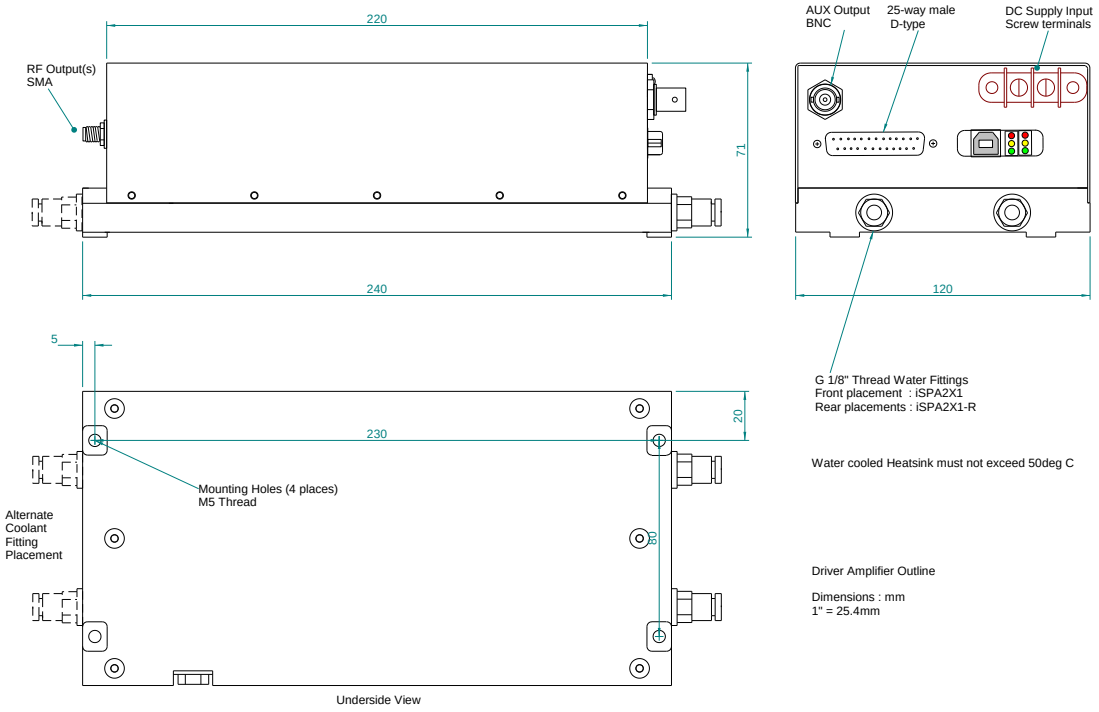


Figure 4: Driver Installation

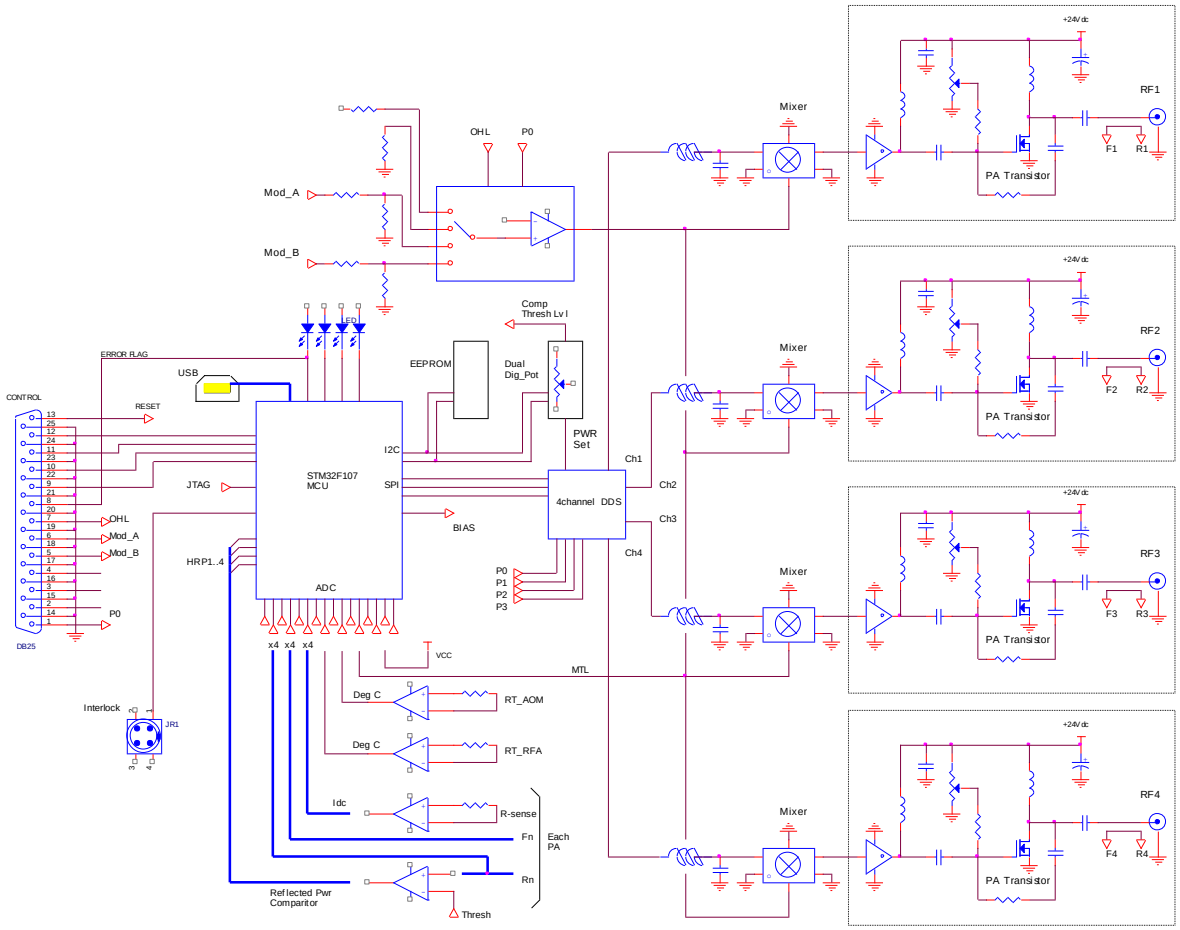
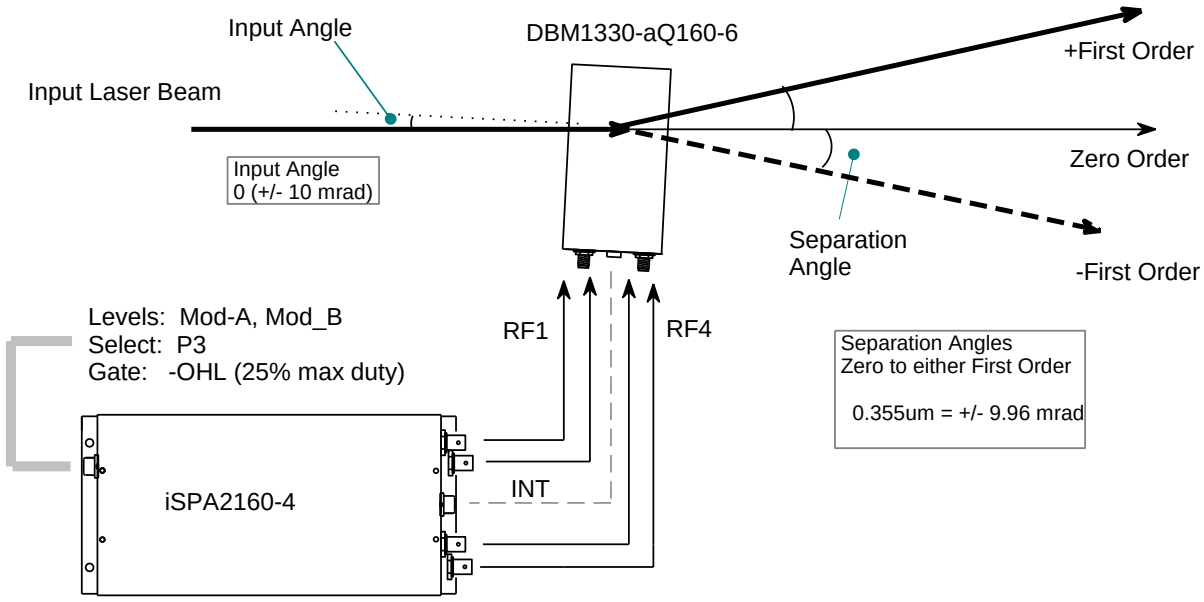


Figure 5: Driver Block Diagram



Coolant circuit not shown for clarity.
Flow rate > 1 liter / min at less than 20deg C

DC supply : 24Vdc / 4A

The separation angle between the Zeroth order and either First order is:

$$\theta_{SEP} = \frac{\lambda.fc}{v}$$

Optical rise time for a Gaussian input beam is approximately:

$$t_r = \frac{0.65.d}{v}$$

where: λ = wavelength
fc = centre frequency = 160.0MHz (355nm

v = acoustic velocity of interaction material = 5.7mm/usec (Quartz)
d = $1/e^2$ beam diameter

Figure 6: Typical Connection Configuration

Connection options for Beam Steered Dual Beam AO Modulators

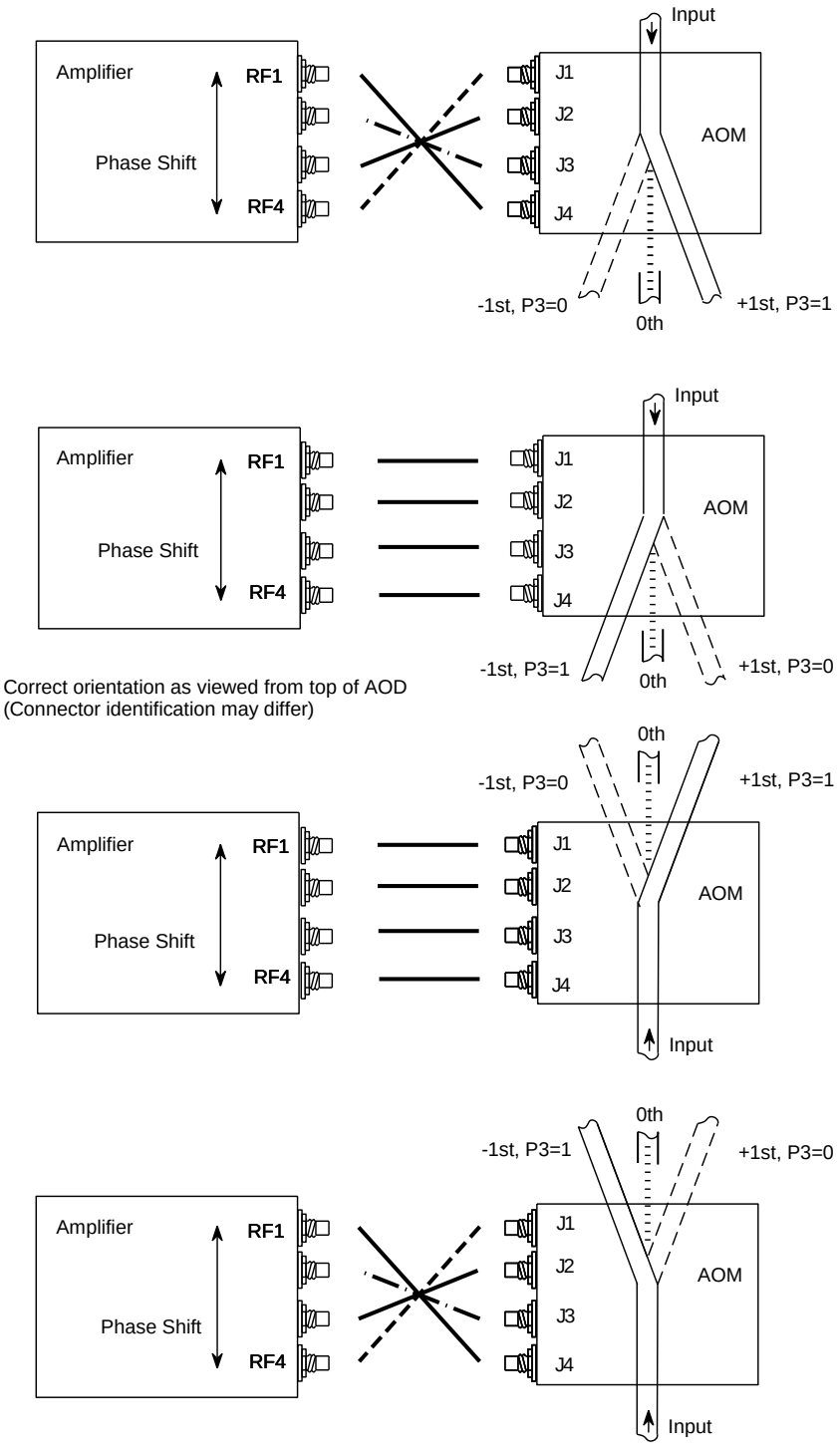
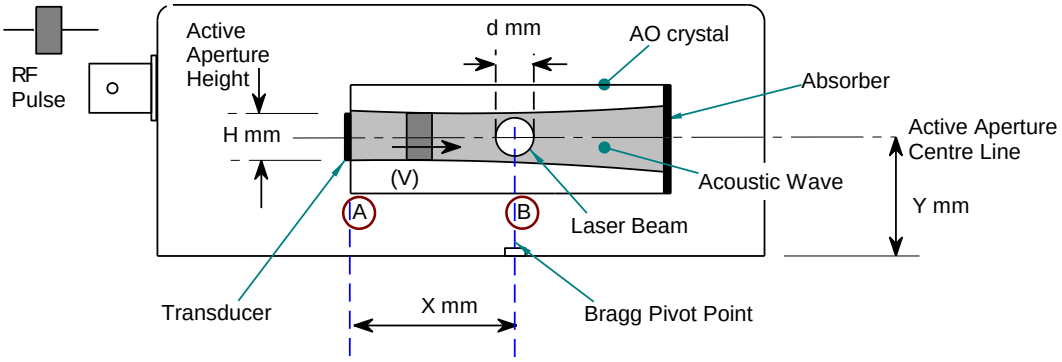


Figure 7. Orientation Options

Appendix A

Pulsed laser, timing considerations

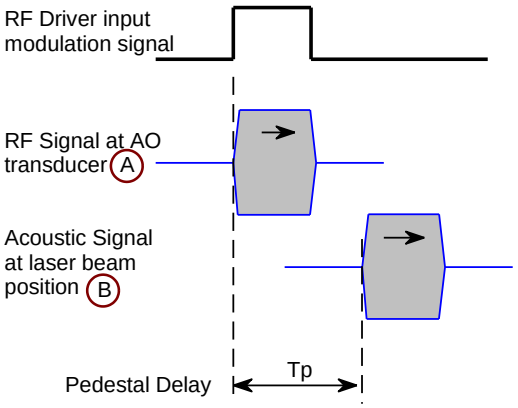
When attempting to synchronize a pulsed laser beam with a pulsed RF acoustic wave in an AO device, the designer must consider the **transit time** of the acoustic wave from the transducer to the laser beam position. This is called the Pedestal delay.



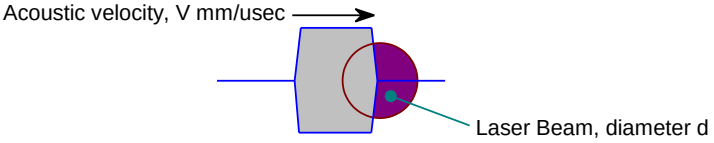
Input Beam Location
Vertical axis: Place the laser beam at the centre of the active aperture at Ymm above the base.
Horizontal (Diffraction) axis : Place beam above the Bragg pivot point.

Timing considerations with respect to the RF modulation signal:
Acousto-optics are travelling wave devices. The acoustic wave is launched from the transducer and travels at velocity V across the laser beam and into the absorber.

1: Pedestal delay = time for the acoustic wavefront to reach the laser beam.
Tp = beam position from transducer (X) / acoustic velocity (V)



2: Transit time = time for the acoustic wavefront to cross the laser beam.
Tt = beam diameter (d) / acoustic velocity (V)
Optical switching time for a Gaussian beam is approximately 0.65 x Tt



Example:

DBM1330 series of UV Quartz AO modulators/deflectors, the Bragg pivot point is located at
X = 3mm from the transducer (+/- 1mm)
The acoustic velocity in Germanium is 5.7 mm/usec

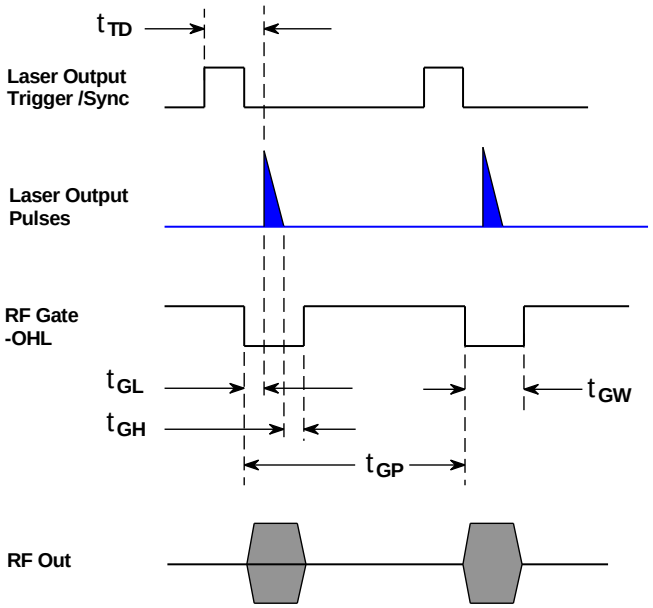
Thus, for a laser beam placed above the Bragg Pivot point
Pedestal delay = 0.53 usec

The pedestal delay will depend on the AO model and the actual laser beam position.

For an 3.5mm input beam diameter, Transit time = 0.61 usec
The optical rise time for a Gaussian beam is approximated by 0.65 x transit time)

Laser synchronization

Please be aware, depending on the Laser type, there may be a significant delay between the laser input trigger signal and the actual laser optical output pulse (t_{TD}).
This should be considered when synchronizing the laser and pulsed RF (acoustic) waves.



Timing	Min	Max
t_{TD}	0	Laser dependent
t_{GL}	AO pedestal delay**	Maximum duty cycle / Laser rep rate * = 10usec *
t_{GH}	0	(Limited by duty cycle)
t_{GW}	0	Maximum duty cycle / Laser rep rate = 10usec *

* For laser rep rate = 25KHz and DBM maximum duty cycle of 20%
** For DBM1330 typical =0.53usec